REMARKS/ARGUMENTS

Pending claims 1-8, 10-11 and 22-24 stand rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,784,331 (Lysinger). Applicants respectfully traverse the rejection. As to claim 1, Lysinger nowhere teaches controlling a sense array to sense multiple word groups simultaneously (i.e., first and second word groups from non-contiguous initial addresses), and controlling the sense array to sense another word group that is twice as large as the first and second word groups. Instead, in Lysinger all that is taught is a conventional manner of sensing data of a single address at a given time. Thus Lysinger describes "in response to the column select signals, a sense amplifier and storage register circuit 712 senses the data from the addressed memory cells and stores that data in respective storage registers." Lysinger, col. 19, lns 19-23. Thus only sensing of a single word group from a first address is performed at a given time in Lysinger.

While Lysinger teaches that data is burst out of storage registers of a sense amplifier and storage register circuit at the same time that address data of another address location is decoded (Lysinger, col. 11, ln. 67 – col. 20, ln. 9), this nowhere teaches or suggests the recited sensing of two word groups from different initial addresses simultaneously. Nor does it teach sensing of different length word groups with a single sense array. Accordingly, claims 1 and 22 and the claims depending therefrom are patentable over the cited art.

For similar reasons, claim 8 is patentable as Lysinger nowhere teaches sensing a first burst length of data at a first initial address that is equal to half of a sense width of a plurality of sense amplifiers of a memory. This is so, as described above instead Lysinger teaches that all of the sense amplifiers operate in parallel to sense data of a full sense width, not a half sense width. Furthermore, Lysinger nowhere teaches sensing a second burst length at a second initial address that is half of a sense width during a latency before reading the first burst length of data. Instead, as conceded by the Office Action, Lysinger teaches that a second access occurs "while data is burst counted out of the memory device" Office Action, p. 5 (citing Lysinger, col. 20, lns. 9-13). Because this second access occurs <u>while</u> data is burst counted out of the memory device, i.e., after a latency before reading the data, claim 8 is further patentable for this reason. Thus claim 8 and the claims depending therefrom are patentable.

With regard to independent claim 18, which stands rejected under 35 U.S.C. §103(a) in view of Lysinger, this rejection is also improper. In this regard, for the same reasons described

above, Lysinger nowhere teaches a sense array that overlappingly senses first and second word groups from first and second initial addresses, or that senses a third word group from a third initial address, where the third word group is twice as wide as the first word group. Instead, as described above, Lysinger merely teaches that "a sense amplifier and storage register circuit 712 senses the data from the addressed memory cells and stores that data in respective storage registers." Lysinger, col. 19, lns. 19-22. Nowhere does Lysinger teach that: its sense amplifier and storage register circuit 712 senses multiple word groups from different initial addresses overlappingly; or senses differently sized word groups (i.e., twice the size of one of the multiple word groups). Accordingly, claim 18 and its dependent claims are patentable.

New independent claim 27 is patentable for similar reasons as described above. Specifically, the cited art nowhere teaches or suggests a sense array that is configurable to overlappingly sense data groups from multiple non-contiguous initial addresses, where each of these data groups are half as wide as a sense width of the sense array, or where the sense array can also sense a data group as wide as the sense array from a different initial address. Accordingly, claim 27 and the claims depending therefrom are patentable over the cited art.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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